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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,300	07/01/2002	Lewis W. Dewey III	BUR920010148	6393

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FREDERICK W. GIBB, III
MCGINN & GIBB, PLLC
2568-A RIVA ROAD
SUITE 304
ANNAPOLIS, MD 21401

EXAMINER

DINH, PAUL

ART UNIT PAPER NUMBER

2825

DATE MAILED: 09/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/064,300

Applicant(s)

DEWEY ET AL.

Examiner

Paul Dinh

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the corresponding address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 July 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 July 2002 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification. Here are few examples.

The specification is objected to because:

- a. Page 5, the same brief description being used for both figures 2 and 3
- b. Page 9, lines 1-6, reference #4 described as both an input (node) and an output (port); according to fig 4, reference #4 is merely an input.
- c. Page 9, lines 1-6, reference numbers 4 and 5 described as both port(s) and node(s) interchangeably; ports are port and nodes are nodes and they are not interchangeable.

Drawings

The drawings have not been checked to the extent necessary to determine the presence of all possible errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the drawings. Here are few examples.

The drawings are objected to because:

- I. The Elements 11, 13, 15, 102 should be labeled according to the functions.
- II. Reference #6 (as described on page 9, line 2) is not shown.
- III. Under 37 CFR 1.83(a), the drawings must show every feature of the invention specified in the claims:
 - Claims 2, 9, 16, and 22 recite "adding resistances of resistors along said path" and "a supply" feature; therefore, the resistances/resistors along path(s) feature and the supply/supplies feature must be shown in the drawings or these features canceled from the claims.
 - Claim 15 recites a comparator; therefore, the comparator must be shown in the drawings or the comparator cancelled from the claim.

No new matter should be entered.

- IV. Besides above-mentioned items I-III, the drawings filed on 7/1/02 are subject to correction of the informalities indicated on the attached "Notice of Draftsperson's Patent Drawing Review," PTO-948. In order to avoid abandonment of this application, correction is required in reply to the Office action. The correction will not be held in abeyance.

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Claim Objections

Claims 2, 9, 16, 22 are objected to because “a supply” is incomplete; the claims should define what kind of supply, i.e., power/voltage supply/source.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claims 4, 6, 11, 13, 18, 20, 24, 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 4, 6, 11, 13, 18, 20, 24, 26 are rejected because “area and perimeter values” are not clearly defined in the specification, drawings and claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Ho (USP 5903469) who discloses a method/system comprising:

(Claim 1 and similarly recited claims 8, 15, and 21)

calculating a minimum output impedance (fig 9-18) for each port (fig 1-5, 8, 25-27);

estimating a maximum parasitic impedance (abstract/background/summary fig 9-18) for each of said ports;

determining an amount by which said maximum parasitic impedance exceeds said minimum output impedance for each of ports (fig 13-16)

extracting actual parasitic impedance values from ports (abstract/background/summary fig 9-18, actual parasitic impedance values from layout) where said maximum parasitic impedance exceeds said minimum output impedance by a determined amount;

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Using said estimated maximum parasitic impedance as said actual parasitic impedance (from layout) for port where said maximum parasitic impedance does not exceeds said minimum output impedance by a determined amount (fig 9-18).

(Claims 2, 9, 16, 22) tracing resistance within each net in a component from a supply (power/ground) a long a least resistive path and adding resistances of resistors a long said path (fig 11-15, c11-14)

(Claims 3, 10, 17, 23) calculating minimum capacitance within each net in said component, considering all bias conditions (fig 11-17)

(Claims 4, 11, 18, 24) c2/7/11, fig 5/12/16-17 teach area and perimeter values of all nets

(Claims 5, 12, 19, 25) geometry of nets (abstract/background summary/fig 5-8/13-16/19)

(Claims 6, 13, 20, 26) summation of area and perimeter values of all said net in said component (fig 1-33)

(Claims 7, 14, 27) calculating a resistance of a total length of wiring having an average width within an associated net within said component (fig 5, 8, 12-15, c7: 56+, c11: 56+, c12: 55+, c13)

2. Claims 1-3, 8-10, 15-17, 21-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Murai (USP 6138267) who discloses a method/system comprising:

(Claim 1 and similarly recited claims 8, 15, and 21)

calculating a minimum output impedance (fig 1-2, 10) for each port (fig 3-9);

estimating a maximum parasitic impedance (abstract/summary fig 1-2, 10) for each of said ports;

determining an amount by which said maximum parasitic impedance exceeds said minimum output impedance for each of ports (120, 204-207 of fig 1-2)

extracting actual parasitic impedance values from ports (abstract/summary fig 1-2, 10, actual parasitic impedance values from layout) where said maximum parasitic impedance exceeds said minimum output impedance by a determined amount;

using said estimated maximum parasitic impedance as said actual parasitic impedance (from layout) for port where said maximum parasitic impedance does not exceeds said minimum output impedance by a determined amount (fig 1-2, 10).

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(Claims 2, 9, 16, 22) tracing resistance within each net in a component from a supply (power/ground) along a least resistive path and adding resistances of resistors along said path (fig 4-8, c8)

(Claims 3, 10, 17, 23) calculating minimum capacitance within each net in said component (fig 1-2, 10), considering all bias conditions (fig 3-9)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is (703) 305-5662. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (703) 308-1323. The fax number for the organization handling this application is (703) 872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Paul Dinh
Patent Examiner
August 28, 2003


VUTHE SIEK
PRIMARY EXAMINER